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[54] **LOGIC PROGRAM COMPARISON METHOD FOR VERIFYING A COMPUTER PROGRAM IN RELATION TO A SYSTEM SPECIFICATION**

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[52] **U.S. Cl.** **395/700**; 364/DIG. 1; 364/280; 364/280.4

[58] **Field of Search** 395/700, 650

[56] **References Cited**

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[57] **ABSTRACT**

It is an object of the present invention to provide a logic program comparison method which makes it possible to do verification by comparing parameterized logic programs and which increases the efficiency of the verification. The keyboard **1** and the input section **4** read two logic programs. The conversion section **5** converts the logic programs into the first and second finite state machine descriptions. The comparison section **6** determines whether there exists an equivalence between the states, between input values, and between output values of the first and second descriptions, and determines whether both descriptions produce respective outputs values deemed equal for all respective inputs deemed equal, for all respective states deemed equal. The result of the comparison is output through the output section **7** and the display unit **2**.

7 Claims, 10 Drawing Sheets